ABSTRACT OF THE DISCLOSURE

An object of the present invention is to enable precise and easy adjustment of clock skew. A clock distribution circuit is designed (S1) and the placement and routing of the entire chip including the clock distribution circuit follows (S2). Then the clock skew value is calculated (S3) and whether the calculated clock skew exceeds a target value is checked (S4). When the clock skew exceeds the target value, the outputs of some driver elements are disconnected or connected to adjust the clock skew (S51). The process of the steps S3, S4 and S51 is repeated until the clock skew becomes equal to or smaller than the target value.